REMARKS

Reconsideration and allowance of the present patent application based on the foregoing amendments and following remarks are respectfully requested.

In the pending Office Action, the Examiner rejected claims 1, 4-8, and 14-16, under 35 U.S.C. §102(e), as allegedly being anticipated by Sriram '227 (U.S. Pat. No. 6,665,227).

By this Request for Reconsideration, no claim has been amended and no new matter has been introduced. As such, claims 1, 4-8, and 14-16 are currently presented for examination.

Applicants respectfully traverse the rejections, under 35 U.S.C. §102(e) for the following reasons:

I. Rejections Under § 102

According to independent claim 1 which recites "selecting either odd ones or even ones of the sample signals during a first slot period to be a first period signal", there are clearly ***more than one sample signals***, whether odd ones or even ones of the sample signals, being selected during the first slot period to be the first period signal. However, Sriram '227 specifically discloses that ***only one FSC signal*** is selected during the first slot period. (*See*, Sriram '227: FIG. 5). There is simply nothing Sriram '227 to suggest that a plurality of sample signals are selected during the first slot period.

Claim 1 also recites "selecting even ones of the sample signals during a second slot period to be a second period signal if odd ones of the sample signals are selected during the first slot period." The claim requires ***more than one sample signals***, even ones of the sample signals, being selected during the second slot period to be the second period signal. Sriram '227 specifically discloses that ***only one SSC2 signal*** is selected during the second slot period. (*See*, Sriram '227: FIG. 5). Again, Sriram '227 fails to suggest that a plurality of sample signals are selected during the second slot period.

Claim 1 further recites "selecting even ones of the sample signals during a third slot period to be a third period signal if odd ones of the sample signals are selected during the second slot period." The claim clearly requires ***more than one sample signals***, even ones of the sample signals, being selected during the third slot period to be the third period signal. But again, Sriram '227 specifically describes ***only one TSC3 signal*** for the third slot period. (*See*, Sriram '227: FIG. 5). Sriram '227 fails to suggest that a plurality of sample signals are selected during the third slot period.

Moreover, according to claim 1, a second period signal is selected from odd ones of the sample signals during a second slot period ***if even ones of the sample signals are selected during the first slot period to be a first period signal***. The Examiner states that the **SSC2** signal of Sriram '227 corresponds to the even ones of the sample signals during the first slot period. In other words, the **SSC2** signal should be the first period signal according to the above recitation from claim 1. The Examiner also states that for the step of "selecting either odd ones or even ones of the sample signals during a first slot period to be a first period signal" of claim 1, the primary synchronization code **508** at time slot **502** (Fig. 5) corresponds to the first period signal. Applicant respectfully disagrees as the **SSC2** signal is ***not identical to the primary synchronization code*** **508**.

Further, claim 1 recites that a second period signal is selected from even ones of the sample signals during a second slot period ***if odd ones of the sample signals are selected during the first slot period to be a first period signal***. The Examiner states that the **SSC1** signal of Sriram '227 corresponds to the odd ones of the sample signals during the first slot period. In other words, the **SSC1** signal should be the first period signal according to the above recitation from claim 1. The Examiner then states that for the step of "selecting either odd ones or even ones of the sample signals during a first slot period to be a first period signal" of claim 1 that the primary synchronization code **508** at time slot **502** corresponds to the first period signal. Once again, Applicant takes issue with this mischaracterization, as the **SSC1** signal ***is not identical to the primary synchronization code*** **508**.

Applicant respectfully submit that the Examiner's inconsistencies continue. For example, claim 1 recites "selecting even ones of the sample signals during a second slot period to be a second period signal if odd ones of the sample signals are selected during the first slot period; selecting odd ones of the sample signals during the second slot period to be the second period signal if even ones of the sample signals are selected during the first slot period." Sriram '227 discloses that one of the even ones of the sample signals is selected during a second slot period to be a second period signal (Fig. 5, **SSC2**) if one of the odd ones (Fig. 5, **SSC1**) of the sample signals is selected during the first slot period. Sriram '227 also discloses that one of the odd ones of the sample signals is selected during the second slot period to be the second period signal (Fig. 5, **SSC1**) if one of the even ones (Fig. 5, **SSC2**) of the sample signals is selected during the fist slot period. Accordingly, both **SSC1** and **SSC2** can be selected as the first period signal. However, ***SSC2, only appears during the second slot period and cannot be found during the first period***. Again, Applicant respectfully regards this as an inconsistency.

In one step of claim 1, a frame synchronization signal is obtained according to the first slot timing and the second slot timing. In other words, ***both the first slot timing and the second slot timing can be referred as the timing information to achieve the frame synchronization***. This is clearly supported by the embodiments disclosed in the Specification which provide that "The slot timings can be obtained by detecting the peaks of the matched filter output." (*See*, Originally-Filed Specification: par. [0008]). However, the timing slot **502** (Fig. 5) and the timing slot **504** (Fig. 5) disclosed by Sriram '227 ***are the physical slots divided in time domain, containing no direct timing information at all***. The "timing slot" is not "slot timing". Applicant respectfully regards this as another mischaracterization.

The inconsistencies and mischaracterizations of the Examiner relative to claim 1 noted above are also seen in independent claim 4. For example, claim 4 recites "a second synchronization unit for obtaining a first frame synchronization signal according to a first slot synchronization signal, and obtaining a second frame synchronization signal according to a second slot synchronization signal", the slot timing for the first slot period is used for the second

synchronization unit to achieve the first frame synchronization and the slot timing for the second slot period is used for the second synchronization unit to achieve the second frame synchronization. Where the slot timing and the slot synchronization signal are both generated from the first synchronization unit. In other words, ***the second synchronization unit obtains two frame synchronization results according to the first slot timing and the second slot timing***.

Sriram '227 discloses that the "***FSC identifies the slot timing*** from the transmitting base station." (*See*, Sriram '227: column 1, lines 63-65). Sriram '227 further discloses that the "first step of the acquisition process includes identification of a base station FSC by a mobile receiver." (*See*, Sriram '227: column 5, lines 44-46; Fig. 7). Sriram '227 also discloses that when "there is no **TSC** code, the mobile receiver need only match one of sixteen code groups and one of sixteen codes within the group for sixteen cyclic shifts of time slots within a frame. In this case, ***the code group match of the SSC provides frame synchronization***."(*See*, Sriram '227: column 5, lines 66-67; column 6, lines 1-4; Fig. 7). The Examiner states that the **SSC** (Secondary Sync Channel, Fig. 5) in Sriram '227 corresponds to the second synchronization unit in the present invention. However, Sriram '227 doesn't disclose that ***the code group match of the SSC can refer two slot timings identified by the FSC to achieve two frame synchronization results***. Therefore the **SSC** is ***not*** identical to the claimed second synchronization unit.

Similar inconsistencies and mischaracterizations are also apparent in the Examiner's analysis of independent claim 14, which recites that ***frame synchronization is achieved by referring to the first slot timing and the second slot timing***. Stated differently, the first slot timing, generated from the slot synchronization process during the first slot period, and the second slot timing, generated from the slot synchronization process during the second slot period, ***are both used for the frame synchronization process***.

Sriram '227 discloses that the "***FSC identifies the slot timing*** from the transmitting base station." (See, Sriram '227: column 1, lines 63-65). Sriram '227 also discloses that the " first step of the acquisition process includes identification of a base station **FSC** by a mobile receiver." (See, Sriram '227: column 5, lines 44-46; Fig. 7). Sriram '227 further discloses that when "there

is no **TSC** code, the mobile receiver need only match one of sixteen code groups and one of sixteen codes within the group for sixteen cyclic shifts of time slots within a frame. In this case, ***the code group match of the SSC provides frame synchronization.***"(See, Sriram '227: column 5, lines 66-67; column 6, lines 1-4; Fig. 7). The Examiner states that the slot sync of Sriram '227 using **FSC** detecting cyclic shift of any of the **N** sequences (Fig. 7) can generate a slot timing for processing the frame synchronization. The Examiner also states that the frame sync (Fig. 7) in Sriram '227 corresponds to the frame synchronization of the claimed invention. However, Sriram '227 fails to disclose that ***the frame sync can refer two slot timings generated from two different slot periods.*** Therefore, the frame sync in Sriram '227 cannot be construed as corresponding to the claimed frame synchronization.

Similar issues exist with the Examiner's analysis of independent claim 15, which recites that ***either the first slot timing or the second slot timing is used for processing the frame synchronization.*** Based on the WCDMA standard, frame synchronization can be completed by determining which of 16 time slots is the first in the frame. The slot synchronization has to be performed first before processing the frame synchronization. Once the beginning timing for each slot is determined first, then the determination of the 16 time slots can be performed. The slot timing obtained from a successful slot synchronization can be regarded a reference to align the beginning timing to each time slot. The Examiner states that the timing slot **502** (Fig. 5), the timing slot **504** (Fig. 5), or the 0.625 milliseconds (Fig. 5) can be regarded as such reference. However, none of them can meaningfully provide the beginning timing of each time slot. Therefore, the timing slot **502** (Fig. 5) and the timing slot **504** (Fig. 5) of Sriram '227 do not correspond to the first slot timing and the second slot timing of the claimed invention and the 0.625 milliseconds does not correspond to the slot timing in the claimed invention.

For at least these reasons, Applicant submits that independent claims 1, 4, 14 and 15 are patentable over the asserted reference. And because claims 5-8 and 16 depend on claims 4 and 15, respectively, claims 5-8 and 16 are patentable by virtue of dependency as well as for

their additional recitations. Accordingly, the immediate withdrawal of the rejections of claims 1, 4-8, and 14-16 is respectfully requested.

CONCLUSION

All matters having been addressed and in view of the foregoing, Applicant respectfully requests the entry of this Amendment, the Examiner's reconsideration of this application, and the immediate allowance of all pending claims.

Applicant's representative remains ready to assist the Examiner in any way to facilitate and expedite the prosecution of this matter. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

Please charge any fees associated with the submission of this paper to Deposit Account Number **03-3975**. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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